

FIG. 1

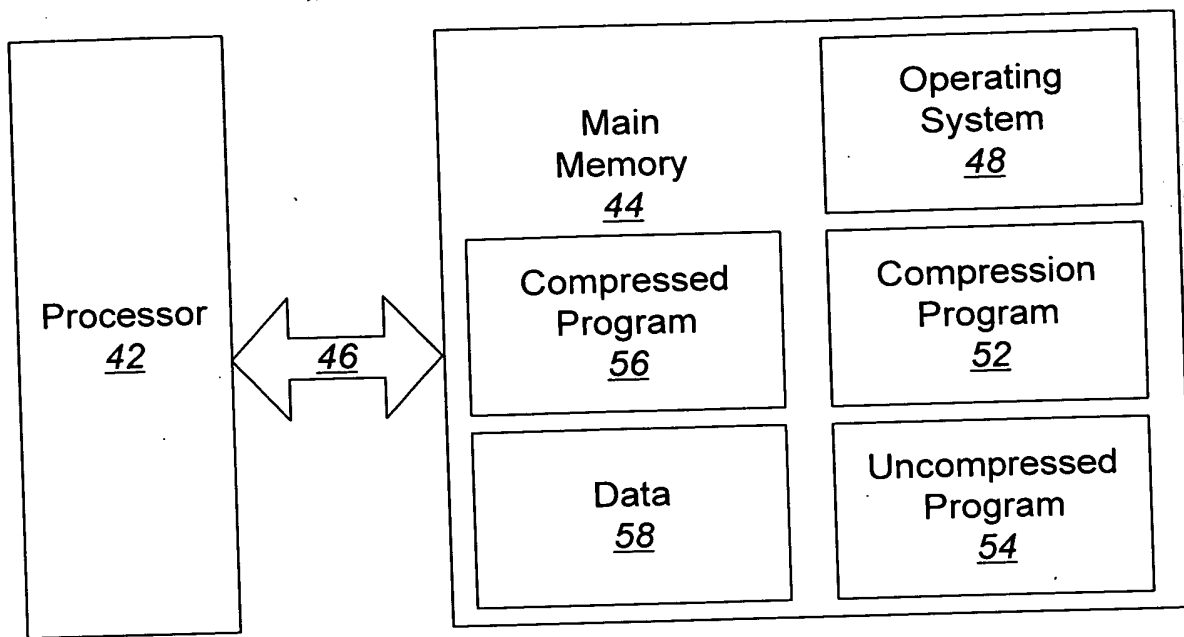


FIG. 2

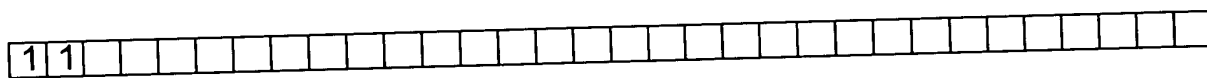
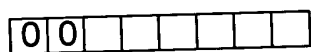


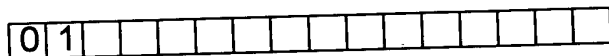
FIG. 3A

Uncompressed Instruction



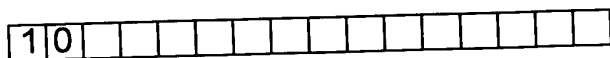
Type I Compressed Instruction

FIG. 3B



Type II Compressed Instruction

FIG. 3C



Type III Compressed Instruction

FIG. 3D

FIG. 4 is a block diagram of a data structure 58a. The data structure 58a is divided into three main sections. The top section is labeled "Third Frequency Count Data Structure (L Instructions) 68". The middle section is labeled "Operand Frequency Count Data Structure(s) (K Operands) 70". The bottom section is labeled "'Jump' Address Data Structure 66". The bottom section is further divided into two sub-sections: "First Frequency Count Data Structure (N Instructions) 62" and "Second Frequency Count Data Structure (M Instructions) 64".

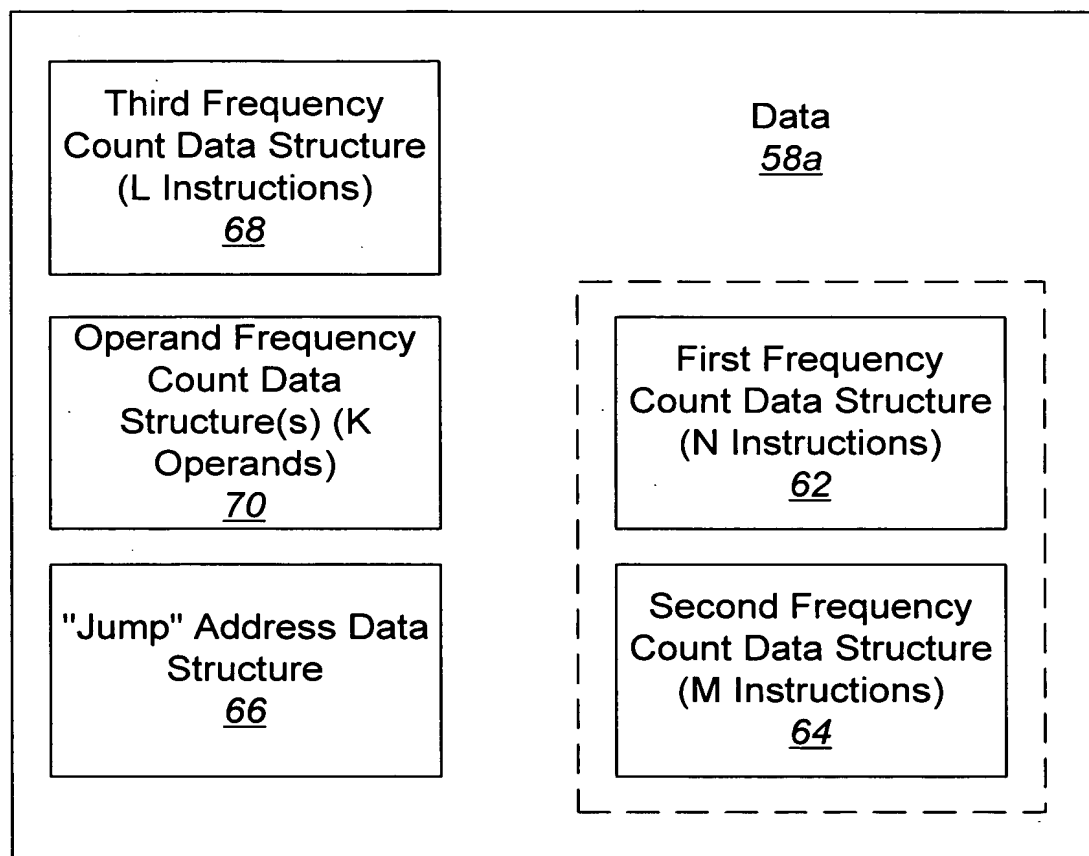


FIG. 4

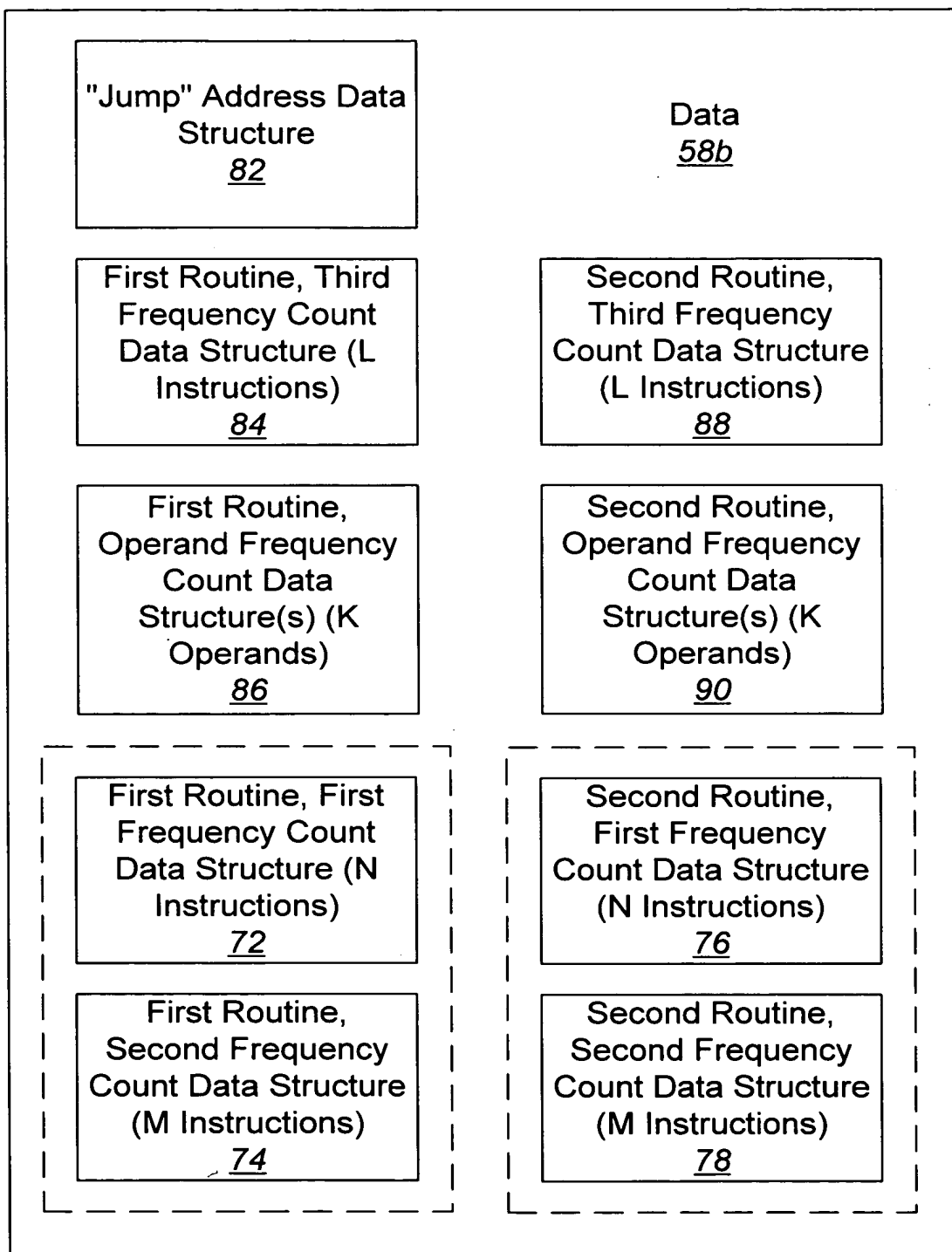


FIG. 5

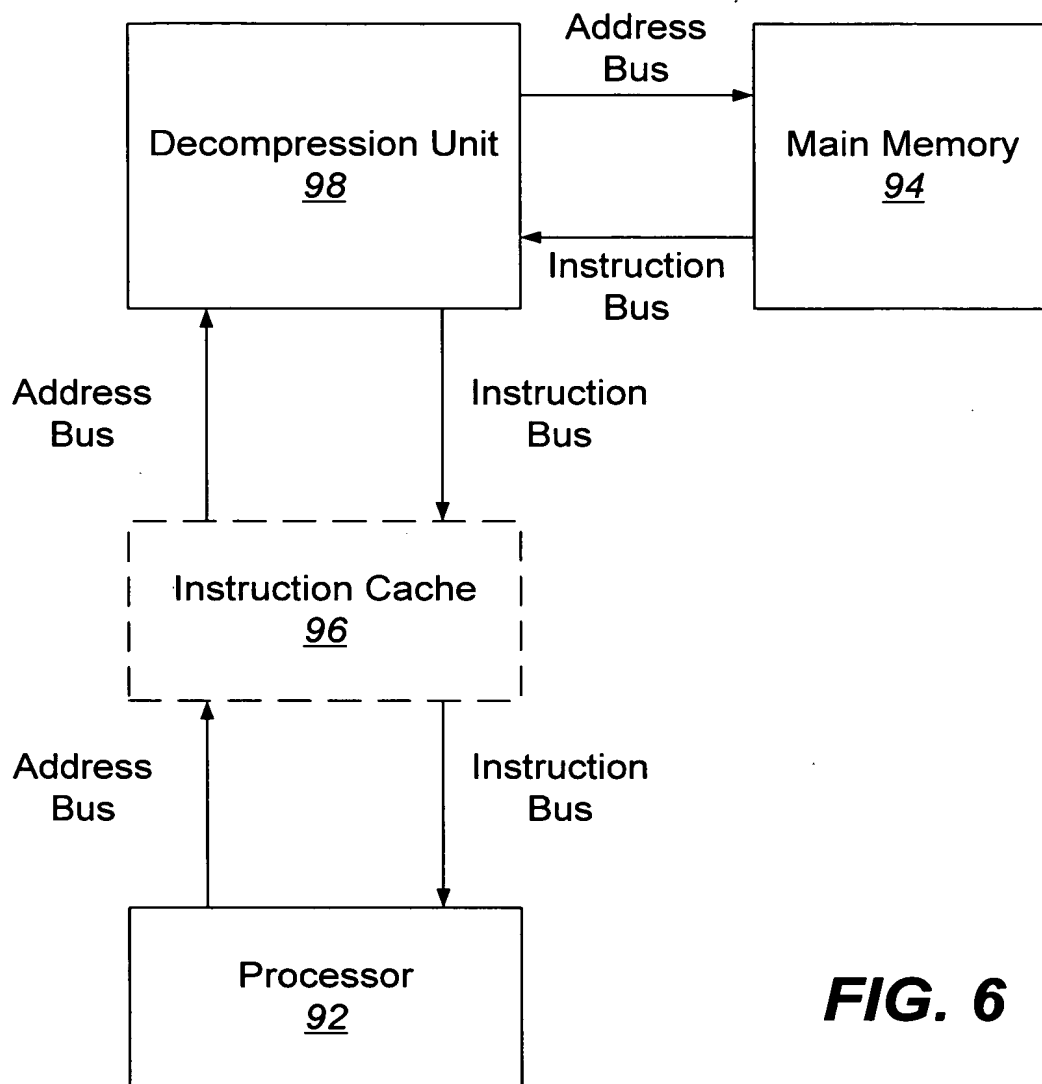


FIG. 6

FIG. 7 is a block diagram of a system architecture for instruction processing, showing the flow of data and control signals between various components.

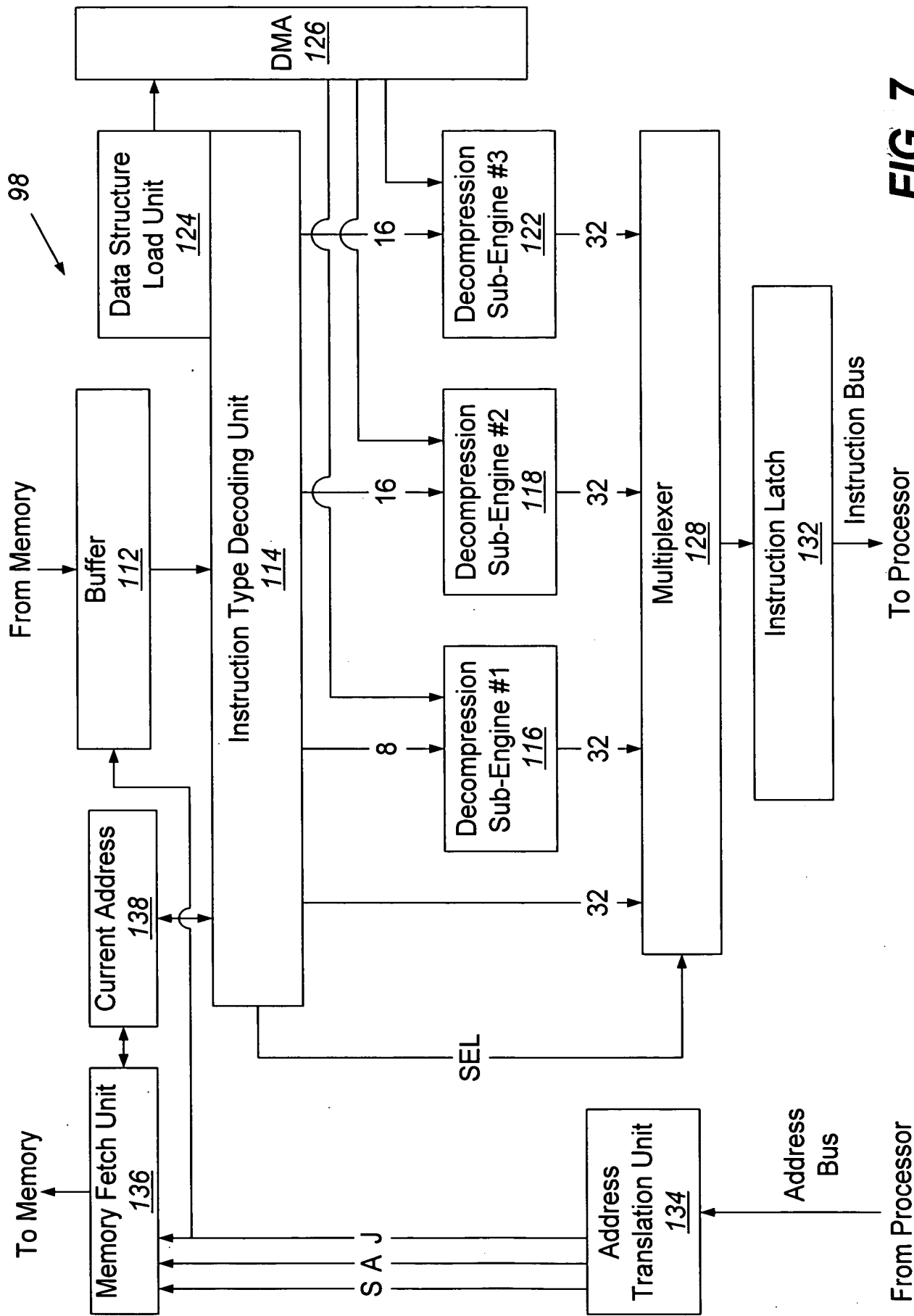


FIG. 7

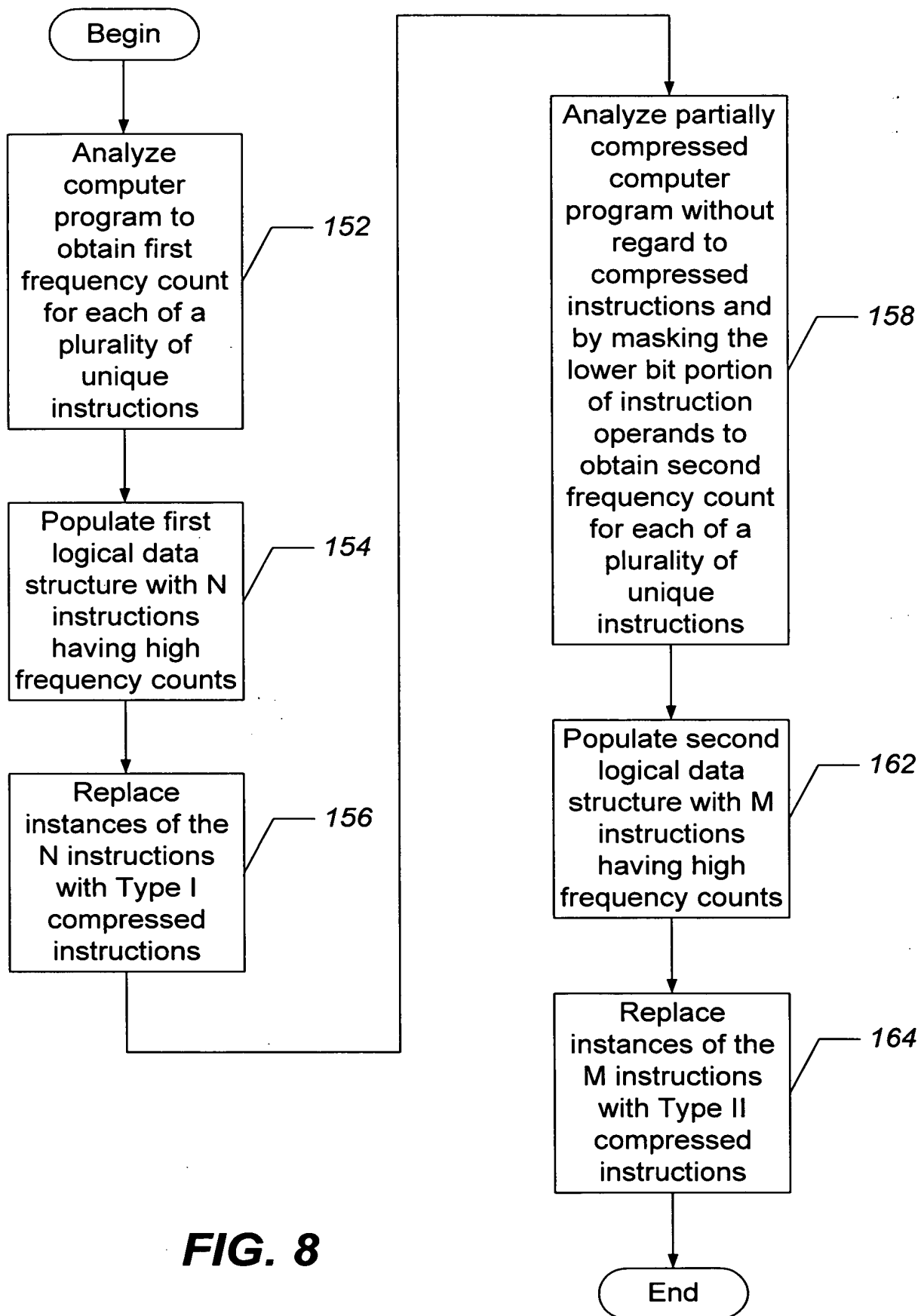


FIG. 8

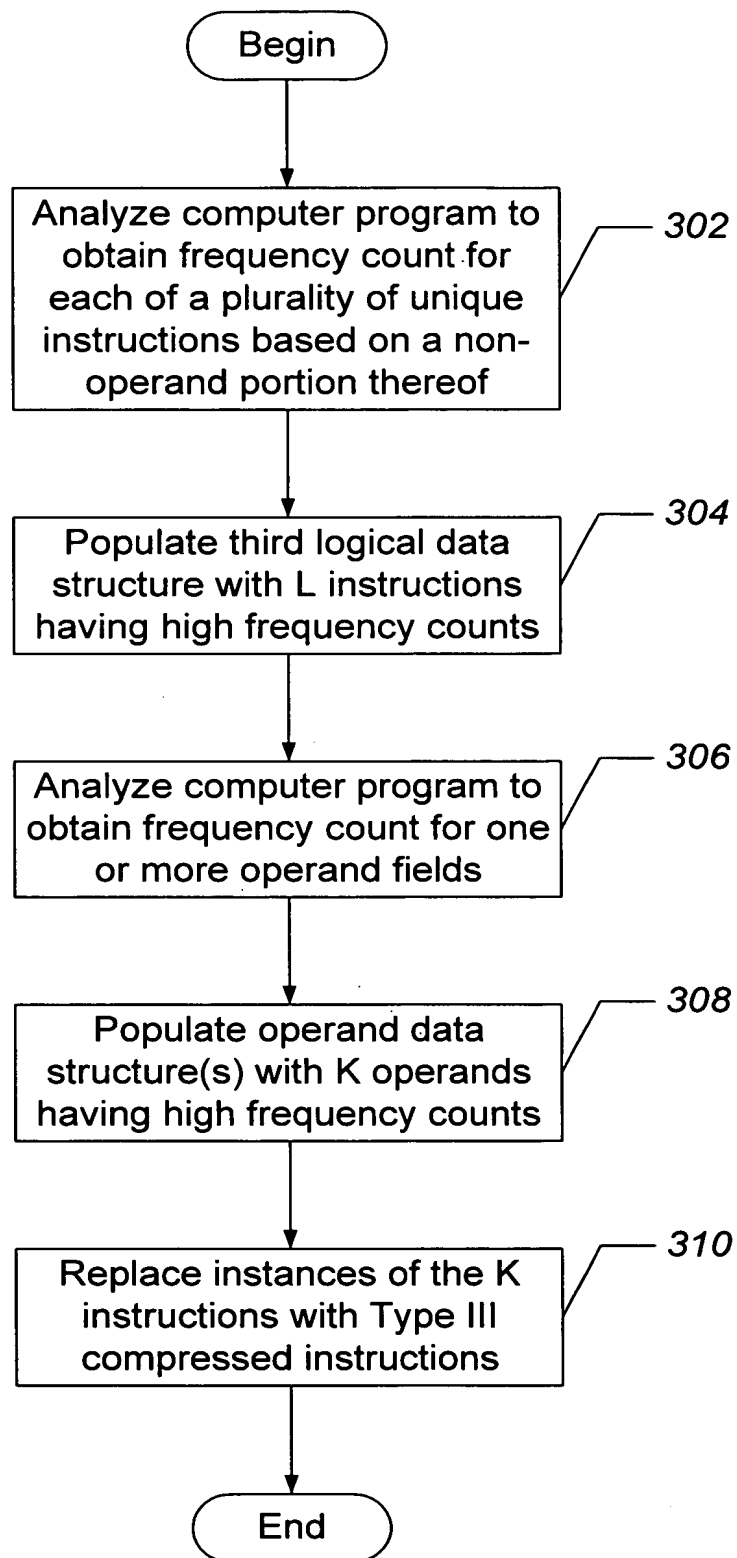


FIG. 9

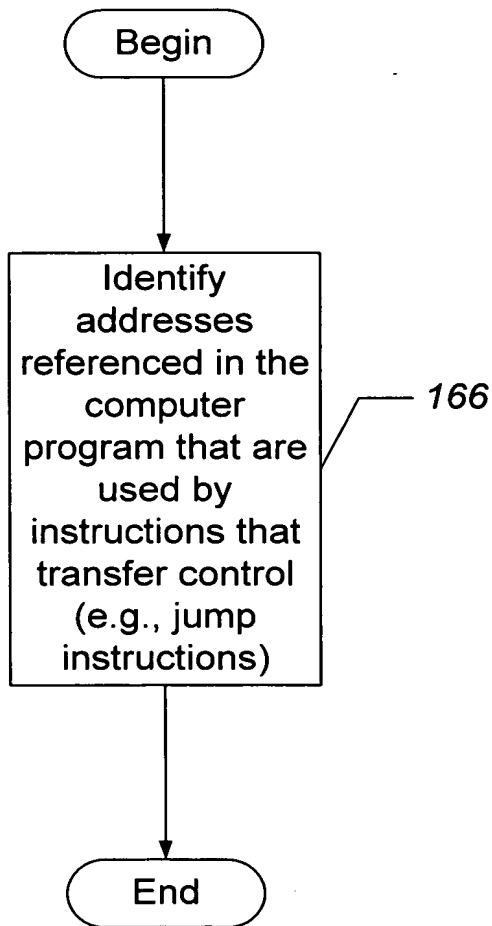


FIG. 10

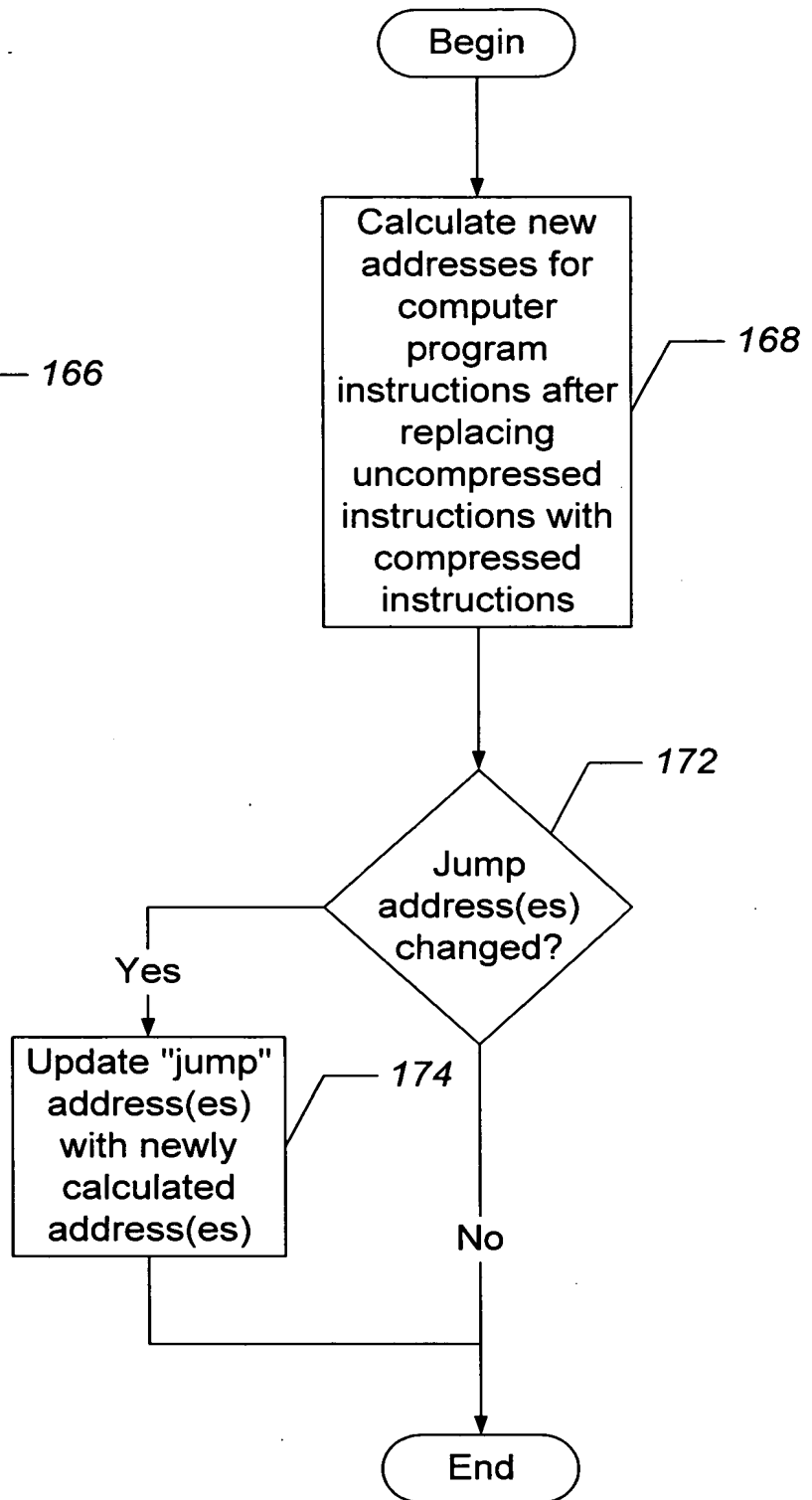


FIG. 11

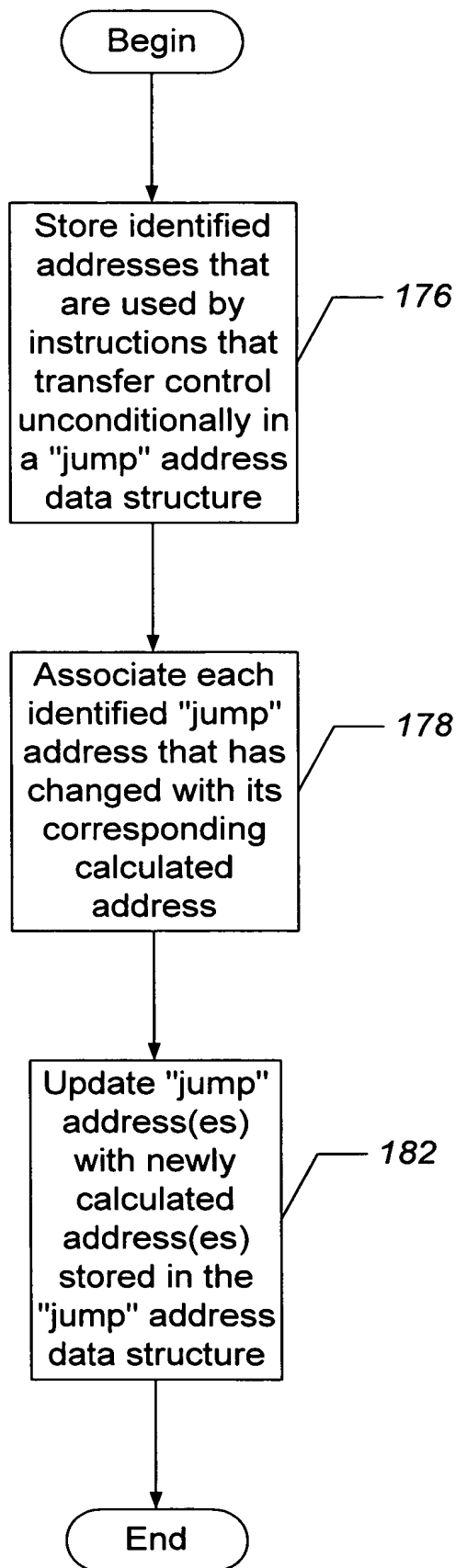


FIG. 12

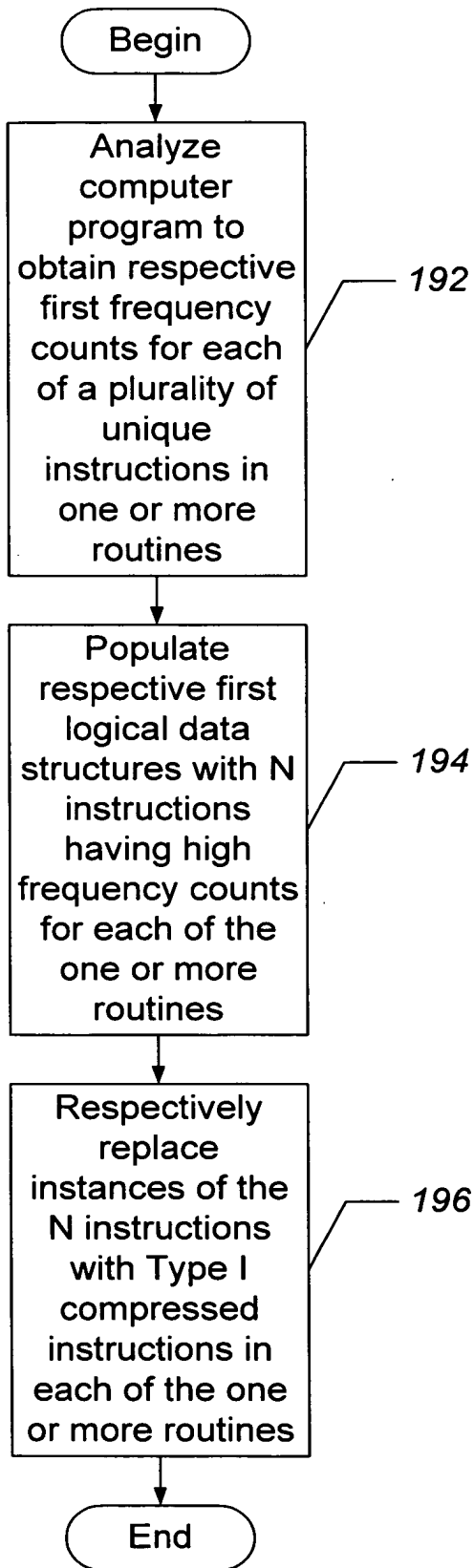


FIG. 13

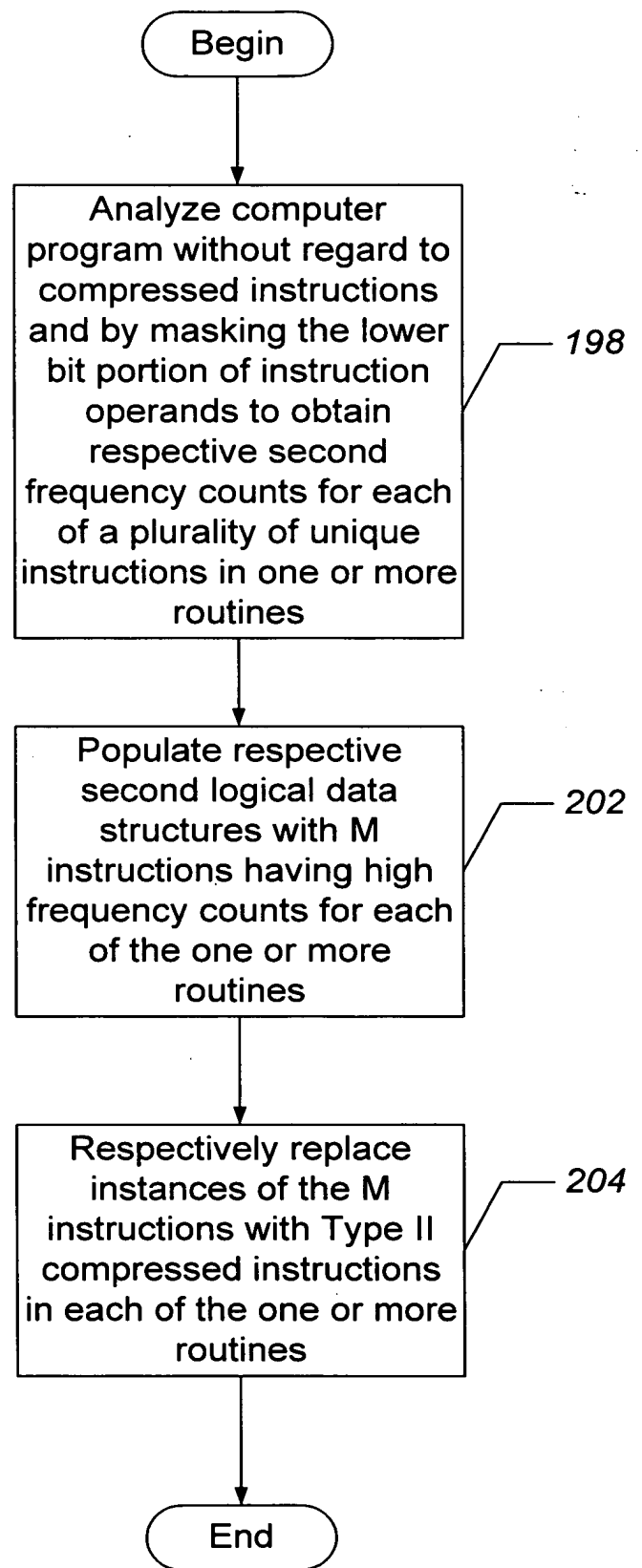


FIG. 14

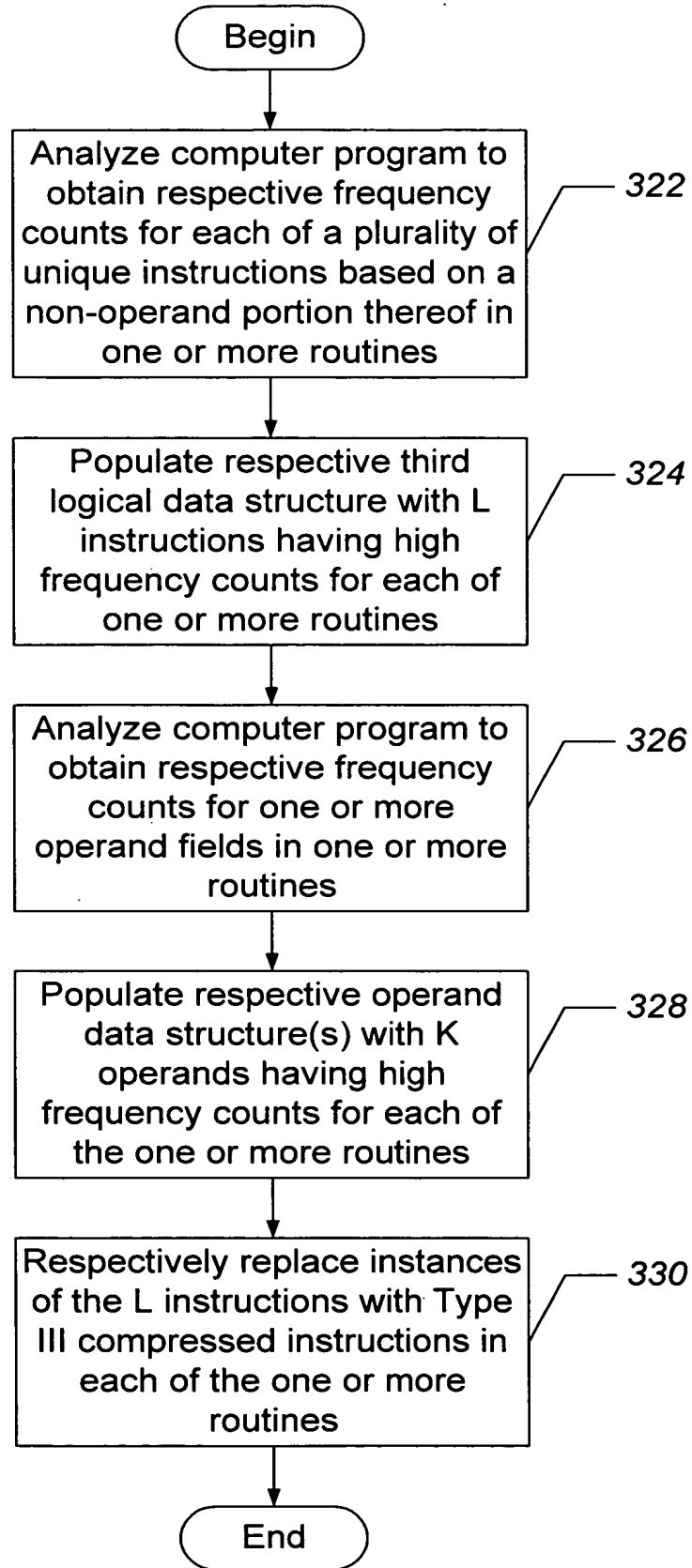


FIG. 15

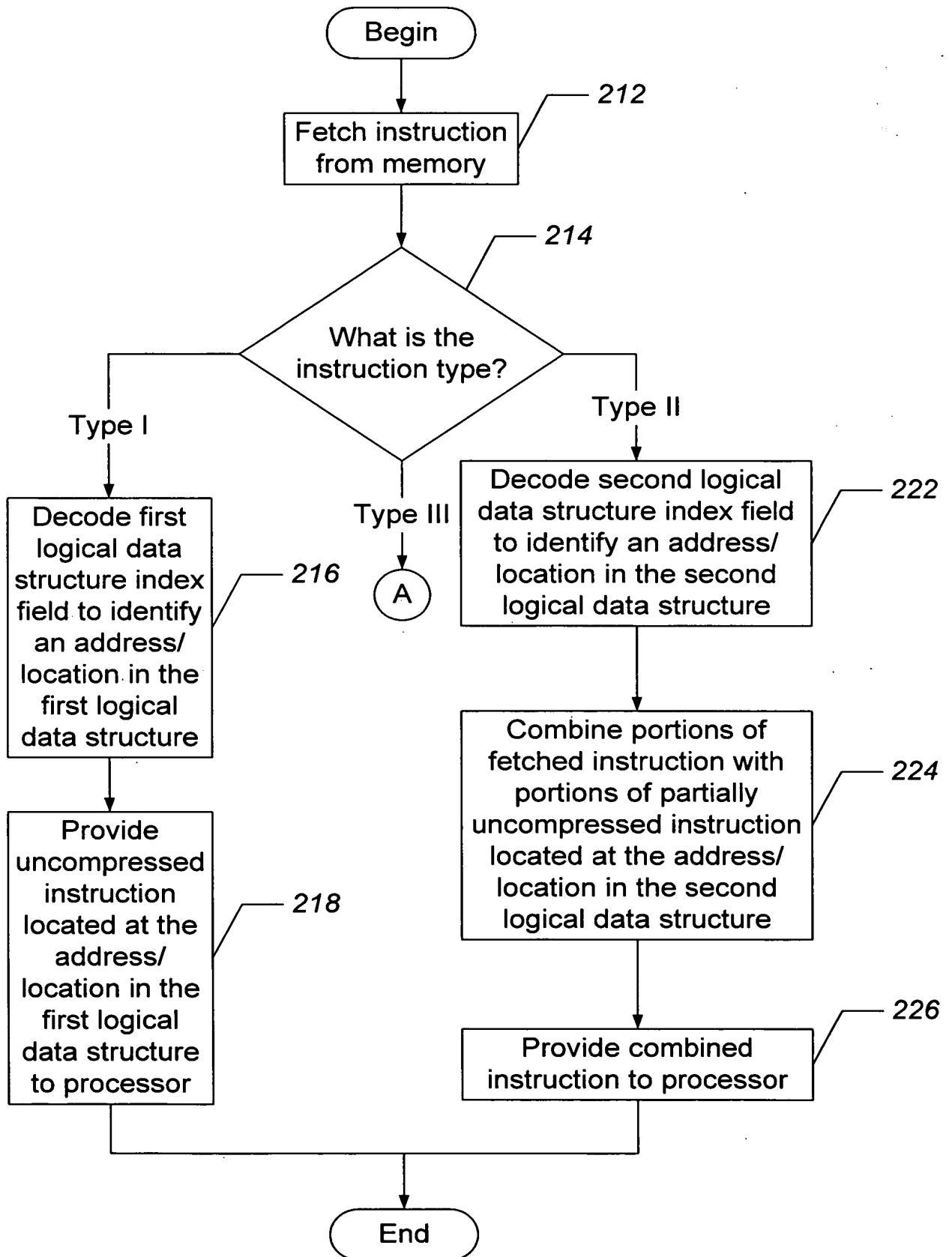


FIG. 16A

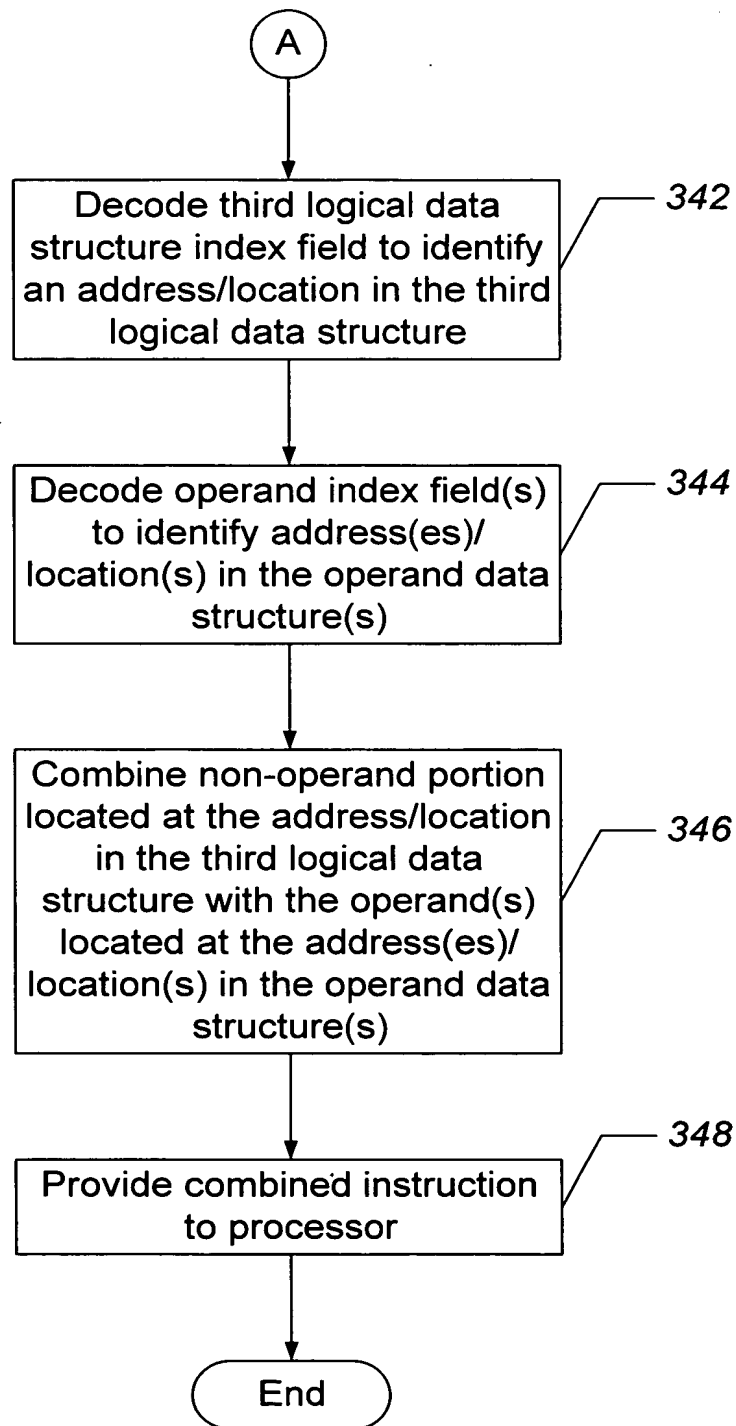
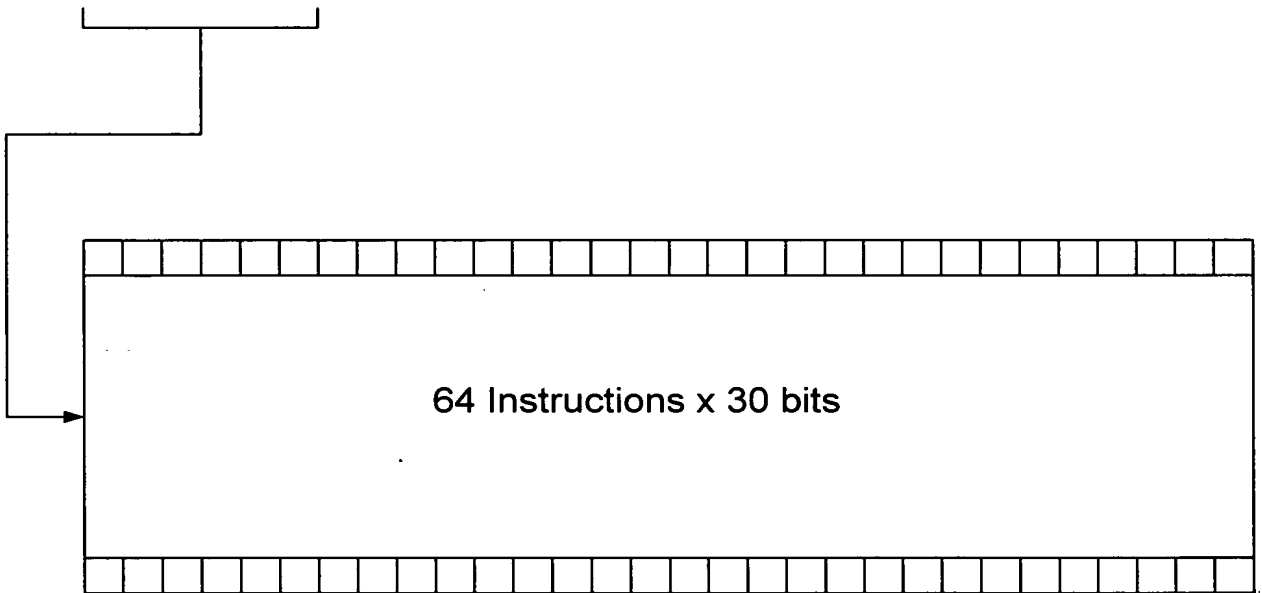
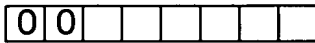


FIG. 16B

Type I Compressed
Instruction



Uncompressed
Instruction

FIG. 17

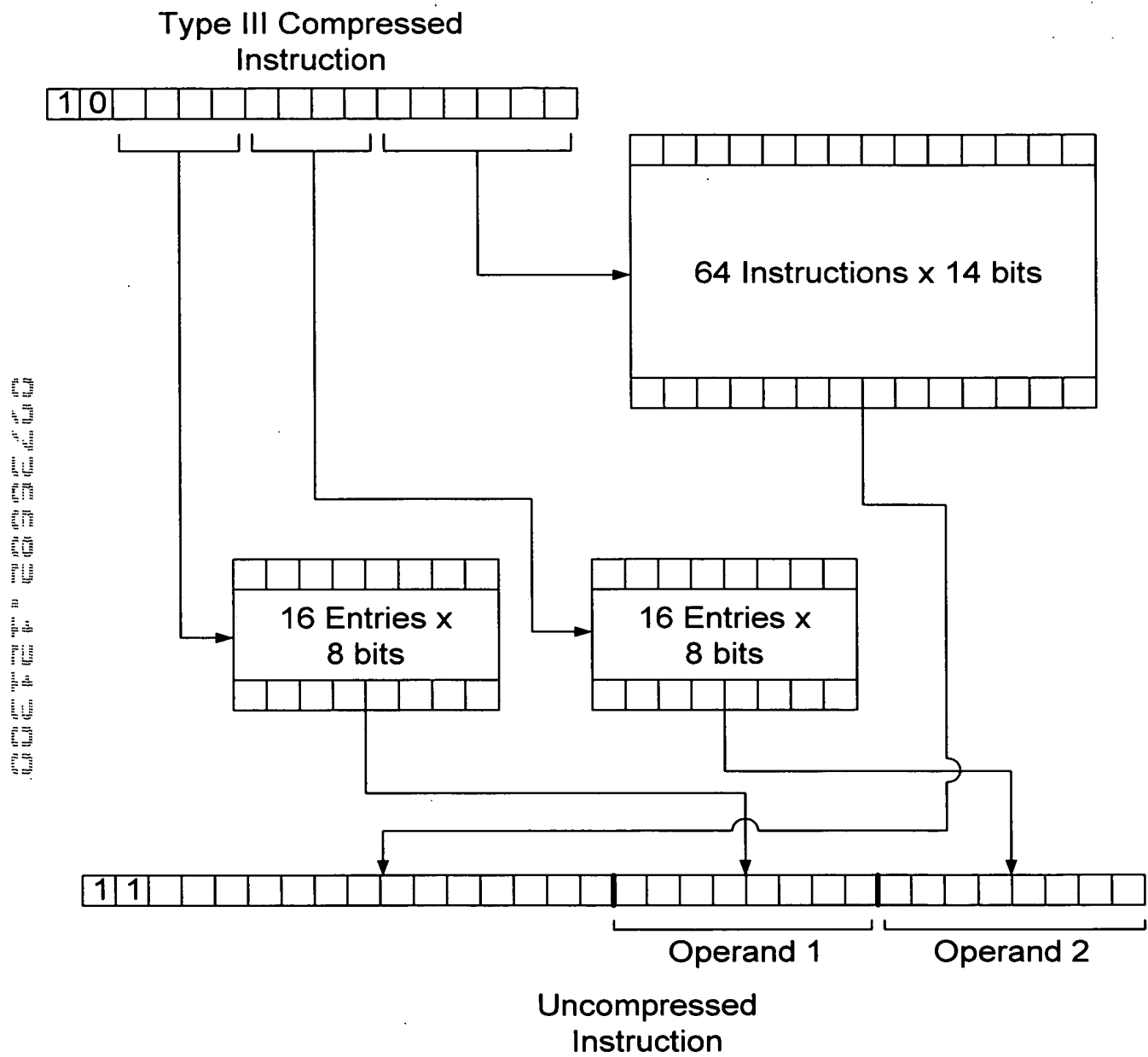


FIG. 19

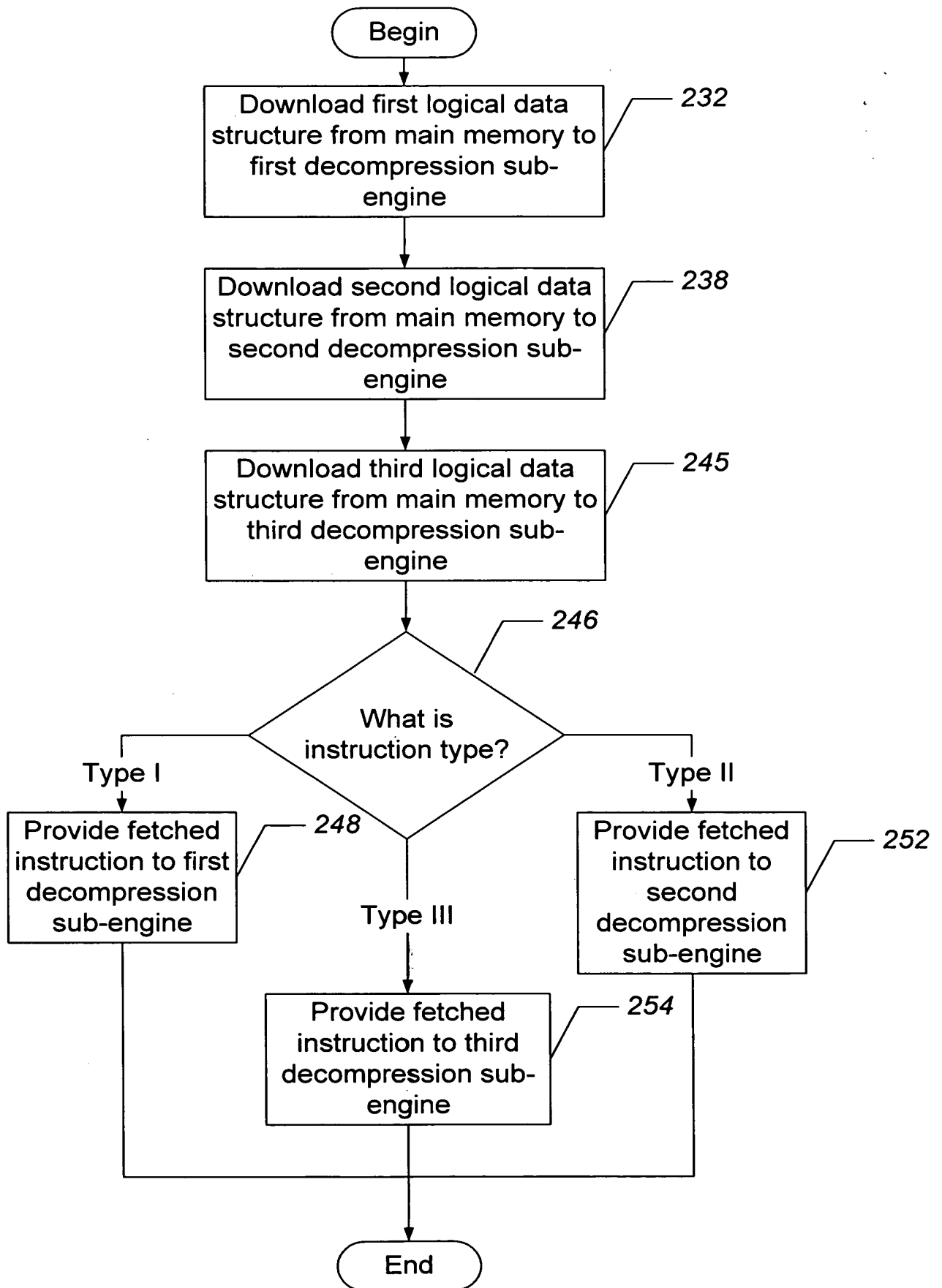


FIG. 20

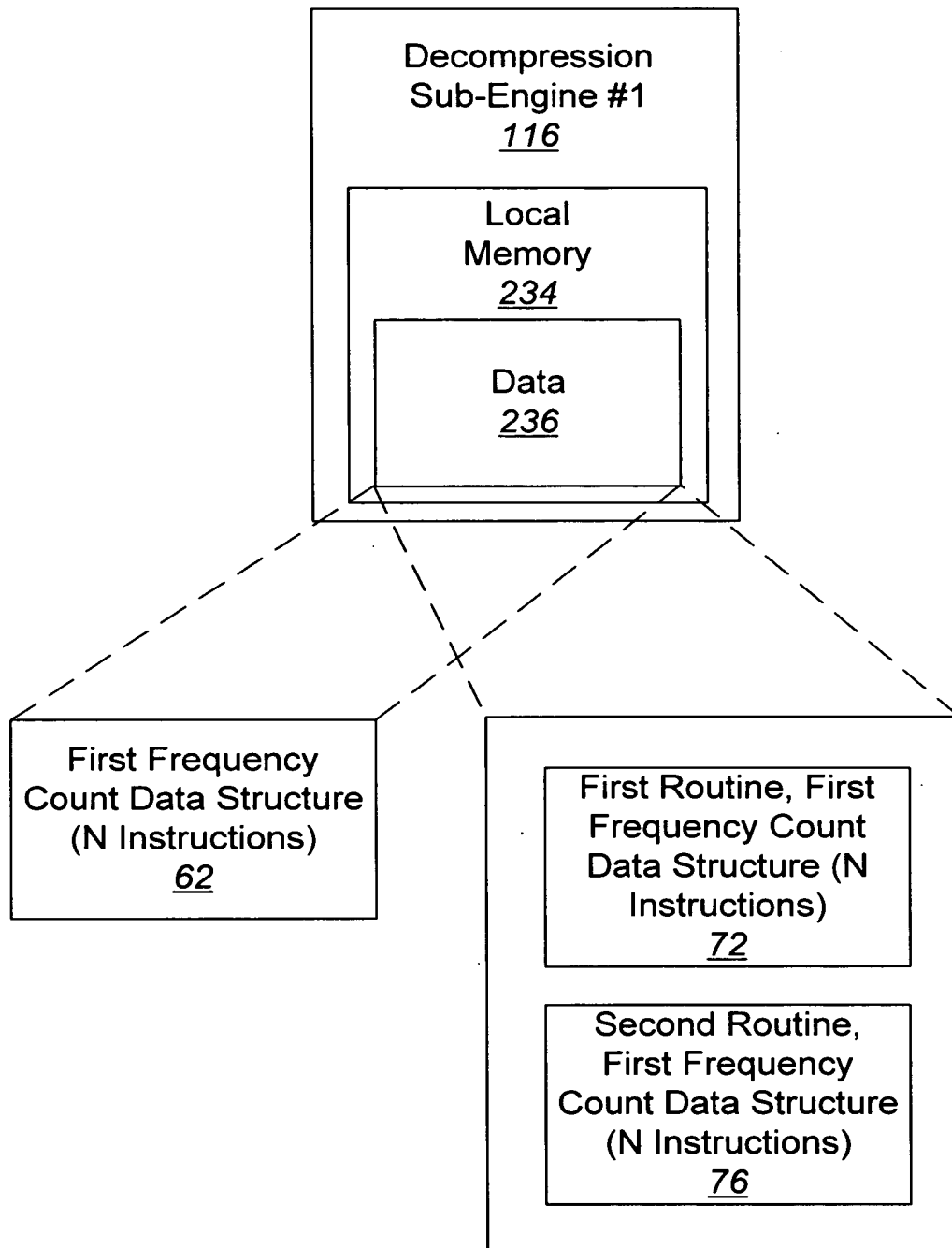


FIG. 21

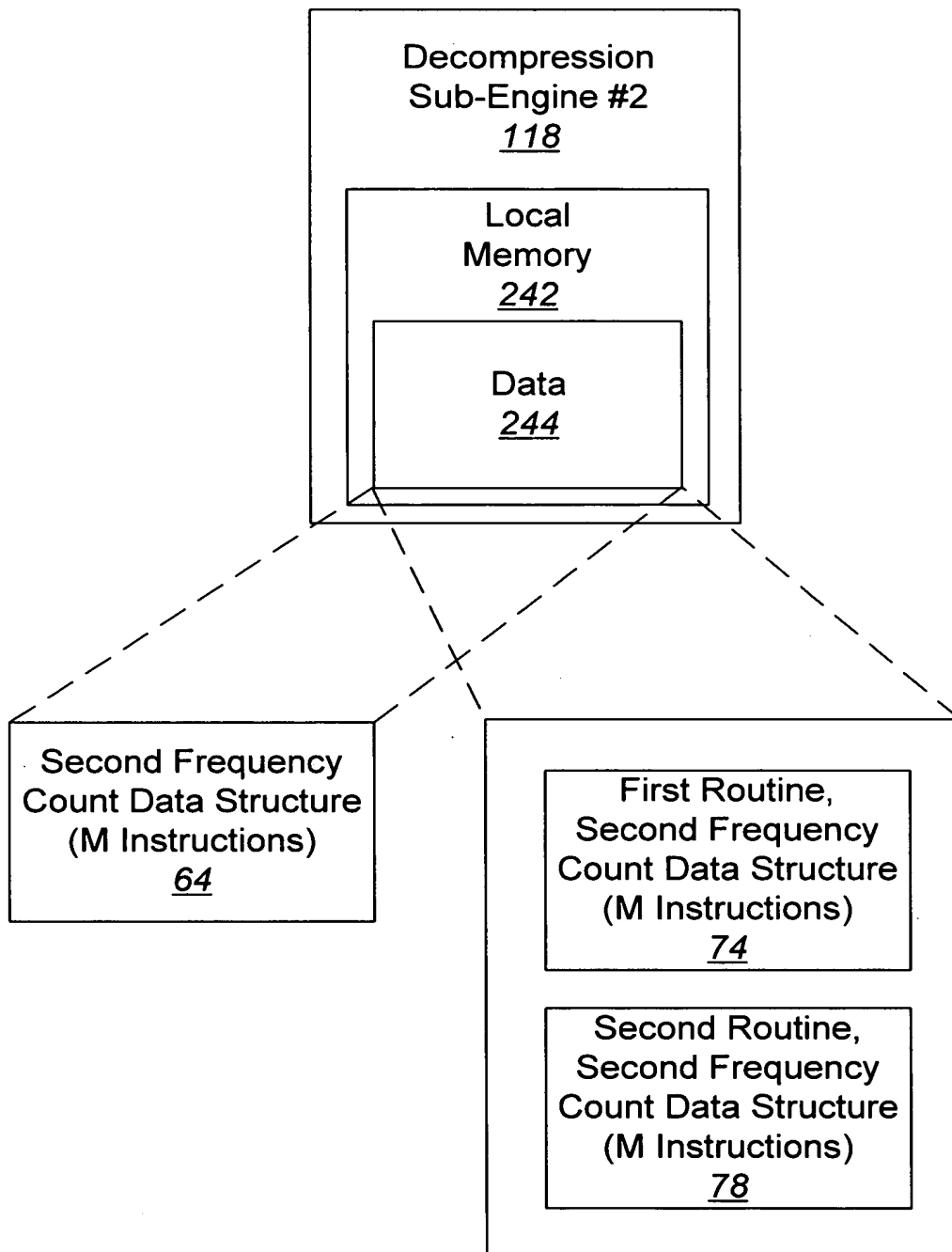


FIG. 22

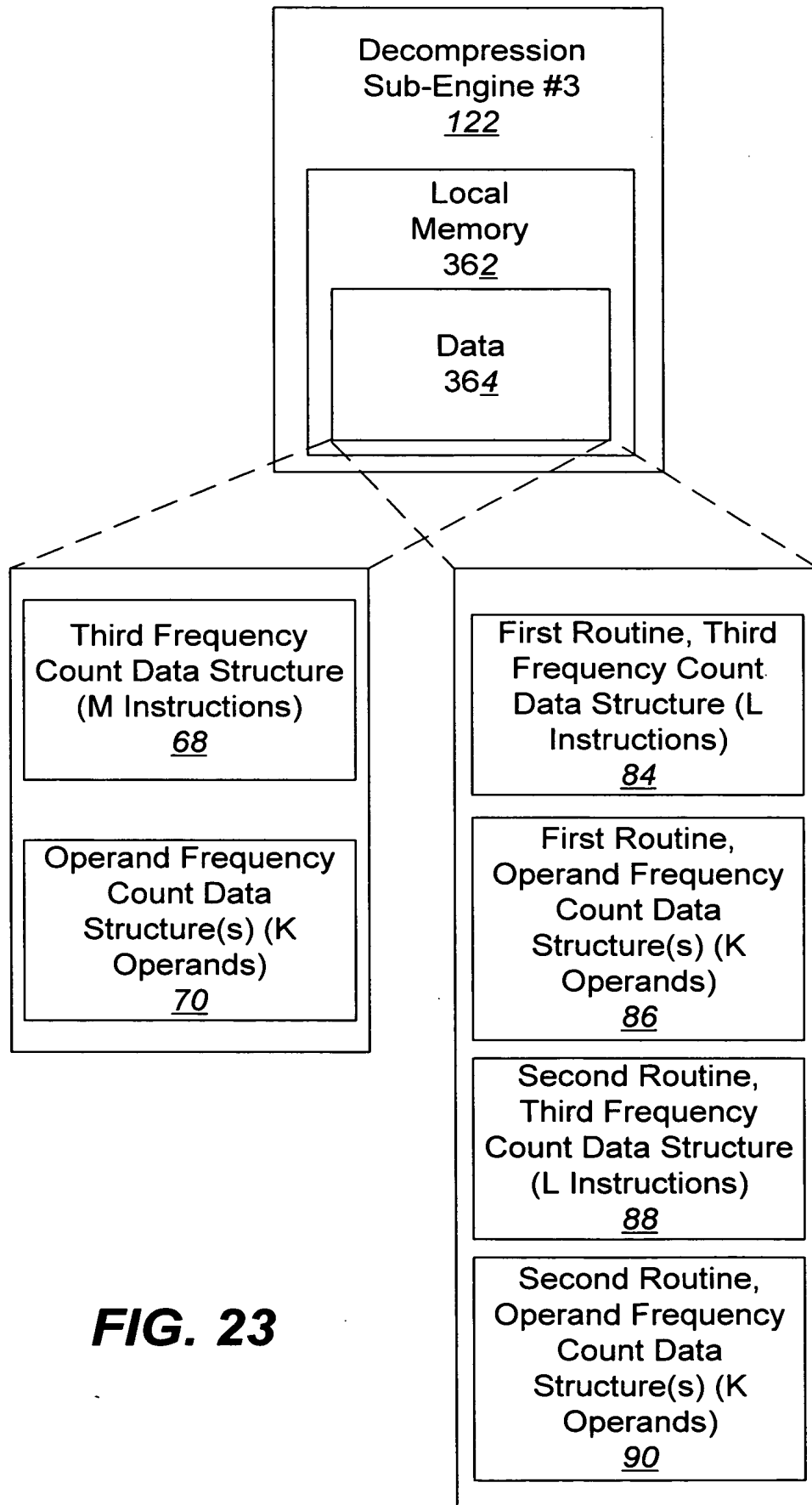


FIG. 23

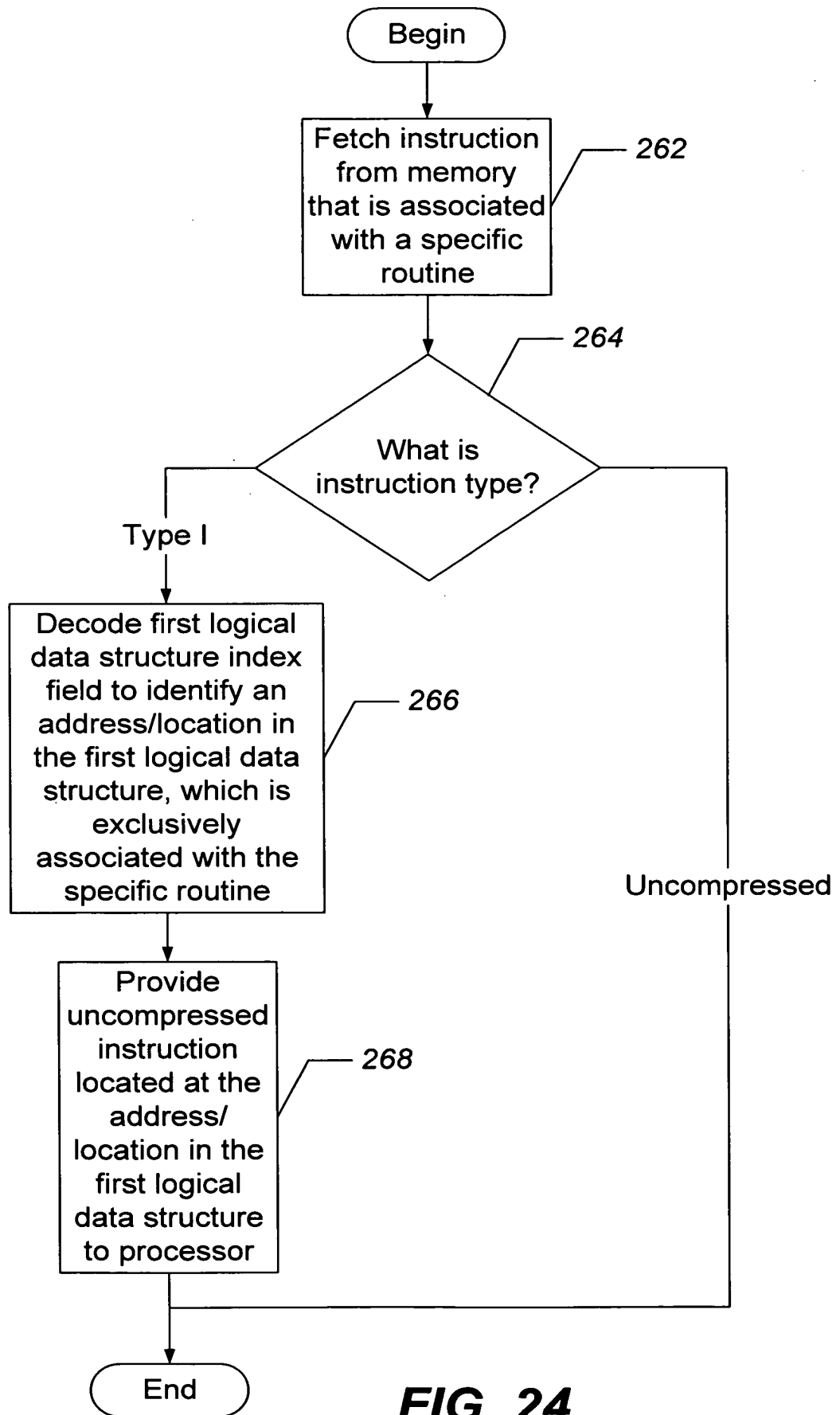


FIG. 24

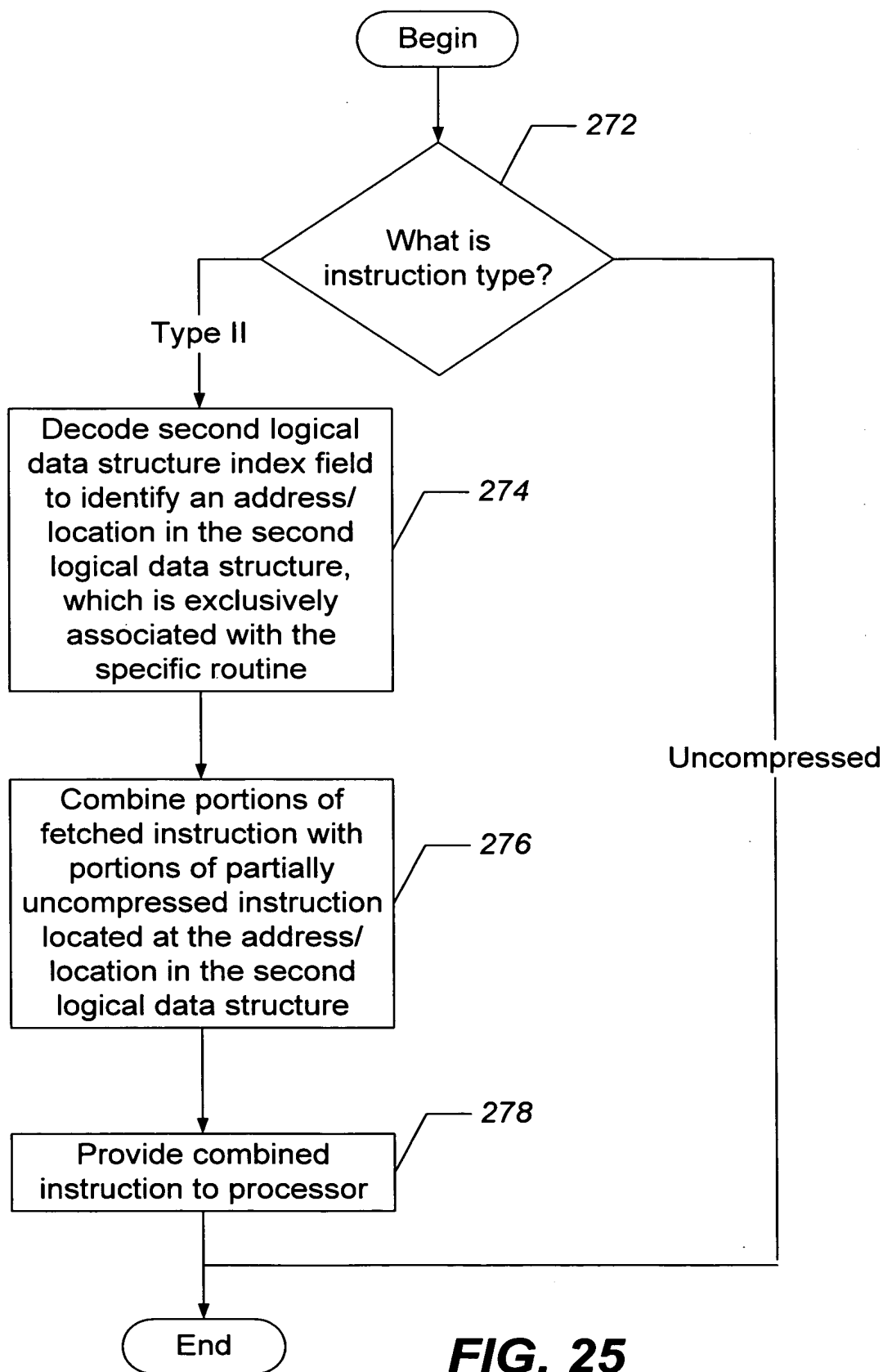


FIG. 25

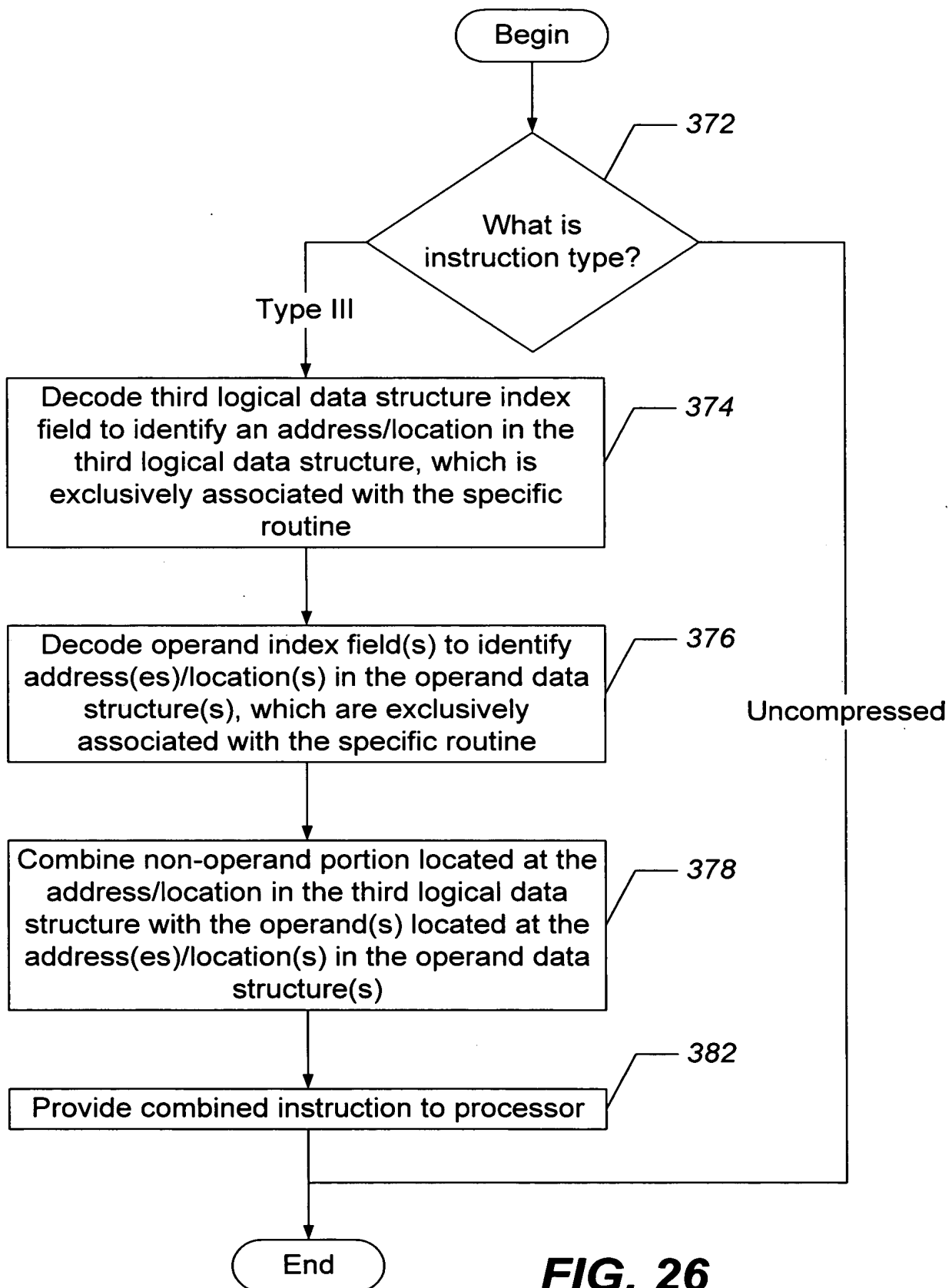


FIG. 26